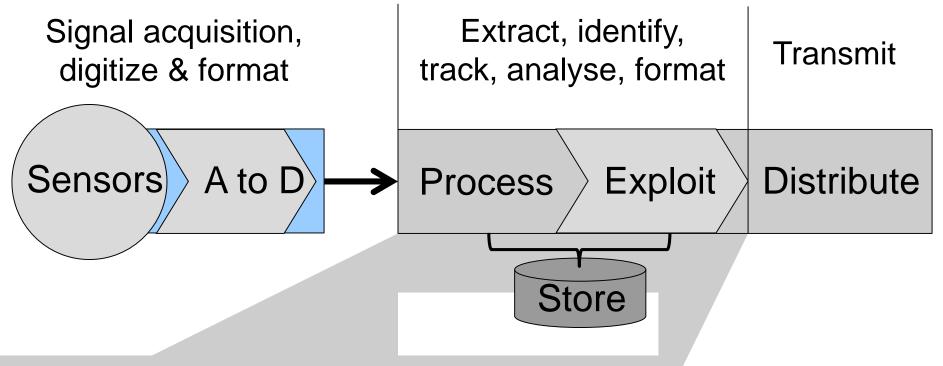




Addressing RADAR Processing needs with 3U OpenVPX COTS Solutions

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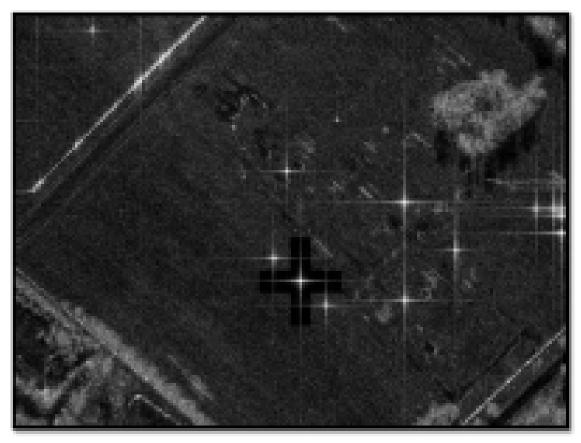
Platform trends – Back end processing



- 1. Multi-core and many-core (GPP, GPU) processing
- 2. High bandwidth, low latency IPC & storage
- 3. Open System Architectures (OSA), standard APIs, middlewares and performance libraries

= <u>HPC clusters</u>

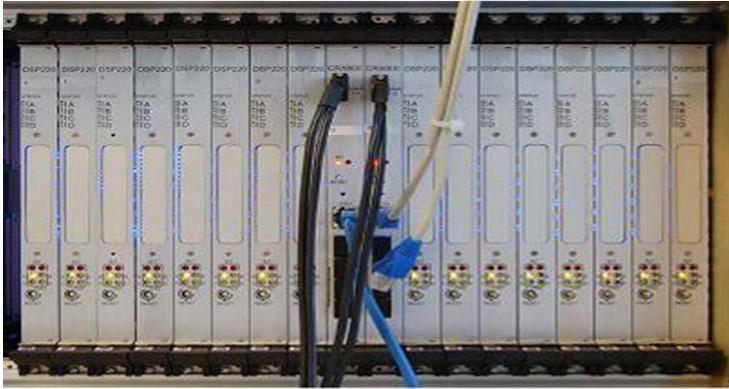
SAR and GMTI applications present significant processing challenges







Legacy high-performance air-cooled system



>3 cu ft., 105 lbs., 2000W



576 GFLOPS peak

Intel[®] Xeon[®] Processor D-1500 Platform Overview

Intel® Xeon® Pro D-1500 Fami	
Broadwell Cores	x8 PCIE2 x8 PCIE2 x24 PCIE3 x24 PCIE3 x24 PCIE3
Server Uncore	x4 USB3 x4 USB2 Legacy IOs BIOS
DDR4/3L 128GB Max	x2 10GbE Intel® Ethernet CS Drivers
ECC UDIMM, SODIMM, RDIMM	LAN Drivers OS/VMM Enabling/Testing
Intel® HW Intel® SW	3rd Party HW

CPU

- Up to 16C BDW Xeon[©] SMT (14nm) *
- Targeted TDP ~20W 65W
- Intel® Xeon® Features

Memory

- 2 Memory Channels, 2 DIMMS/channel
- DDR3L/DDR4
- 128GB Max Capacity

Integrated IOs

- x24 PCIE 3.0, x8 PCIE2.0
- x6 SATA3
- x4 USB 3.0, x4 USB 2.0
- x2 10 GbE Intel® Ethernet

Storage/Network Features

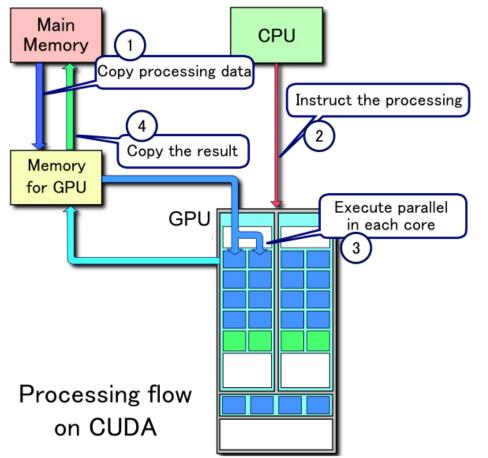
- Storage/Network Environment (Reliability, Temp, Availability)
- Validated with external Crypto accelerator (Coleto Creek)
- Non-Transparent Bridging (NTB), Asynchronous DRAM selfrefresh (ADR), Intel® QuickData Technology

Recent changes in red * 8/12 core Extended Temperature Versions

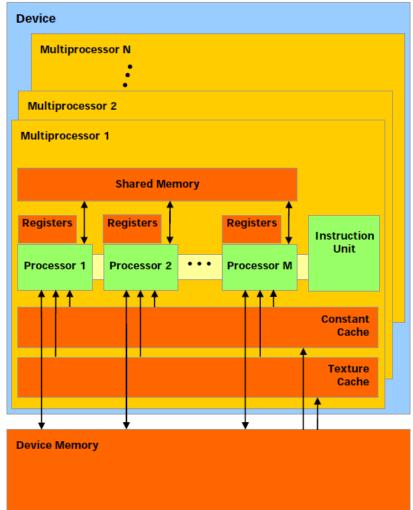
NVIDIA GM107 Maxwell GPU

- Maxwell architecture targets performance/Watt
- 640 cores
- 1.1 TFLOPS (theoretical)
- 128-bit dual-bank memory
- PCI Express Gen 3 (subject to system compatibility)
- 28 nm process technology
- CUDA Compute 5.0
- Shader Model 5.0, OpenGL 4.4, PhysX, DirectX 11.2
- Commercial equivalent is the GeForce GTX 850M

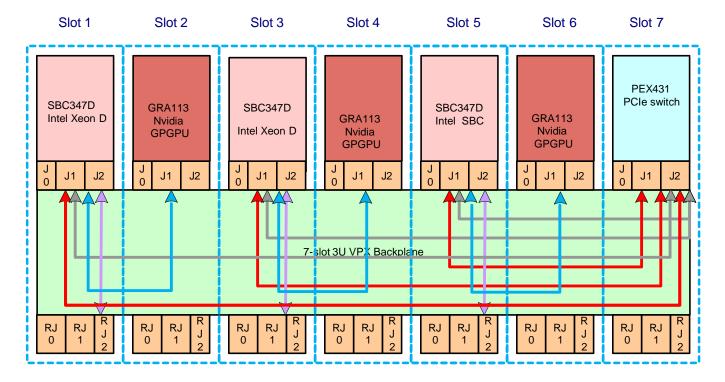
CUDA model



1 Multiprocessor = 8 Processors



Putting it all together in 3U OpenVPX





x16 PCle Gen 3
1000Base-BX ethernet
x4 PCle Gen 3

<1 cu ft., <45 lbs., <500W >4.5 TFLOPS peak

Considerations

- Radar applications such as SAR and GMTI suit CPU/GPGPU combinations
- Throughput on the backplane is trending from PCIe Gen 3 to Gen 4
- and 10 to 40GE
 - 10GBASE-KX4 and 10GBASE-KR with a view towards 40GBASE-KR4
 - Optical Interconnects have to be considered at or above Gen 4 and 40GE
- CPU cores will continue to trend upwards
- Nvidia's next generation Pascal GPGPU will be over 1,000 cores
- 3U OpenVPX is a great way to address SWaP in space/weight constrained environments



